
CSC TTC Subsystem

prepared for ATLAS TTC Review
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CSC TTC subsystem: Overview

CSC = Cathode Strip Chamber subsystem of Muon Spectrometer

- 1st precision measurement in forward & backward directions ($|\eta| > 2$)
- mounted on “small wheel”; operates in high-radiation environment

Two TTC partitions

- Forward & Backward (or “A” and “C”)

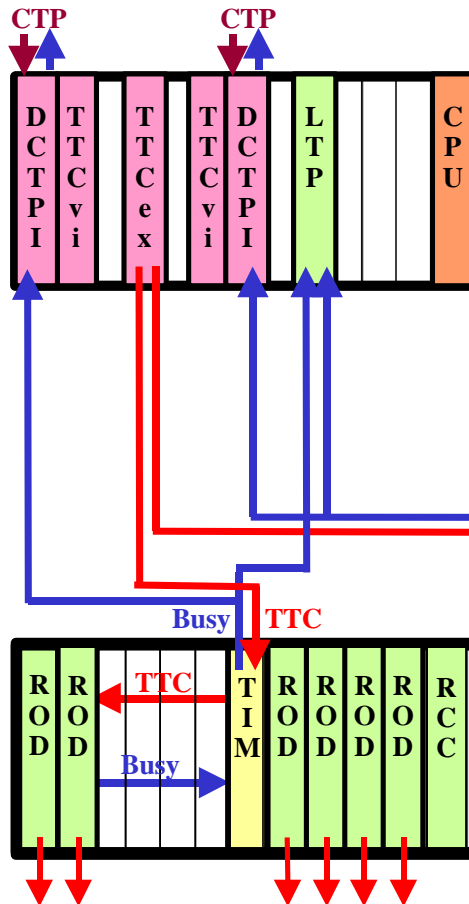
Each partition:

- 1 ROD crate w/ 16 RODs (8 initial + 8 staged) + 1 TIM (Timing Interface Module)
- distribution of timing, trigger, and control signals:
 - CSC TTC crate to TTCrx in TIM via fiber (standard TTC protocol)
 - TIM to RODs via backplane (special protocol)
 - RODs to chamber-mounted signals via fiber (clock & readout control signals only)
- collection of Busy signals:
 - RODs to TIM via backplane
 - TIM to Busy module in CSC TTC crate via cable

Standalone operation for electronics calibration:

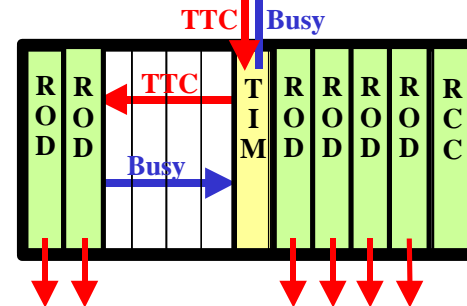
- TIM provides all control signals required for electronics calibration
- RODs collect and reduce calibration data

CSC TTC subsystem: Layout of TTC modules

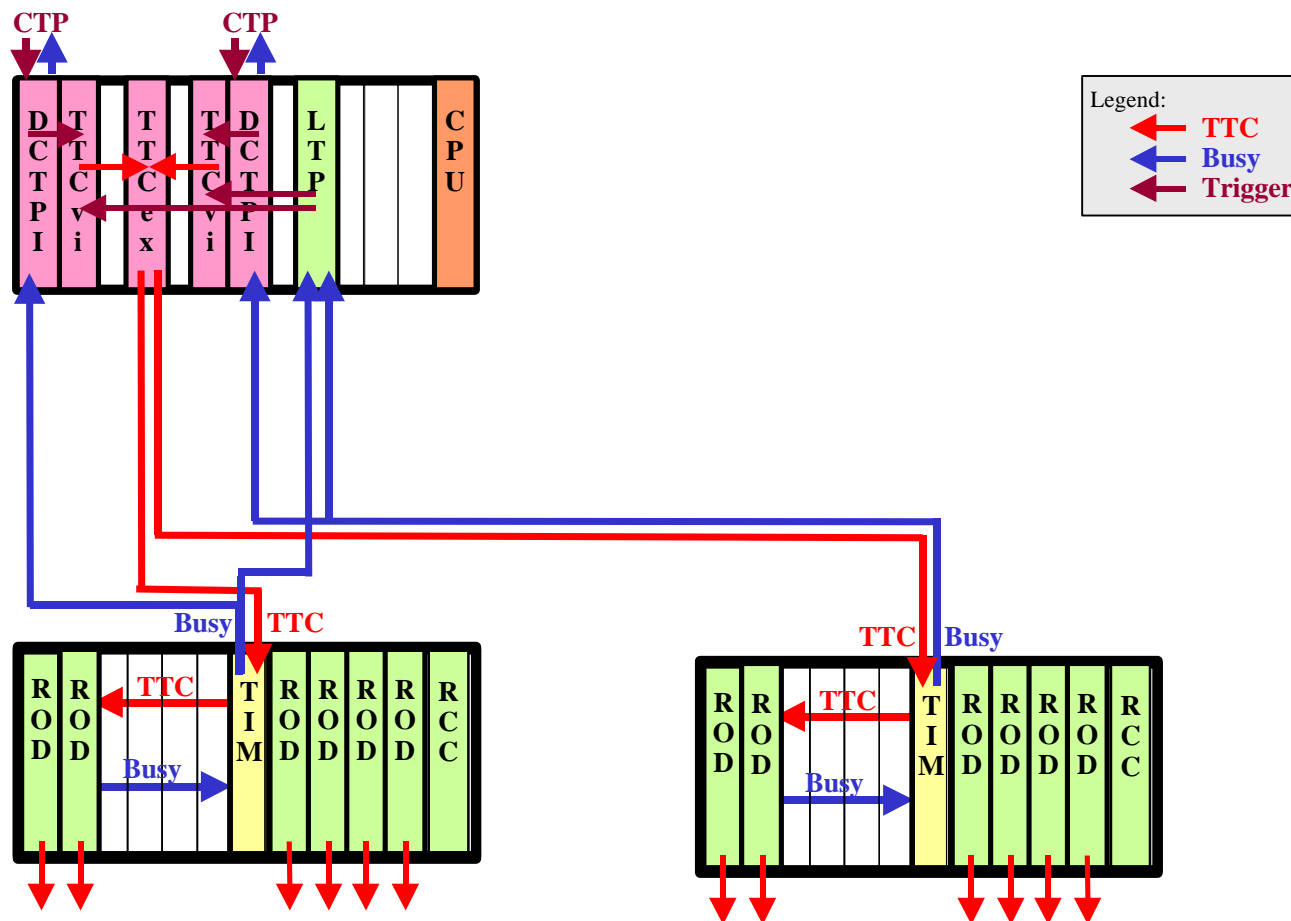


Materials list:

- 1 TTC crate (6U VME)
- 1 single-board computer
- 2 TTCvi
- 1 TTCex (w/ attenuators)
- 2 DCTPI
- 2 fibers (TTCvi to TIM)
- 2 TTCrm (in TIMs)
- 2 TIM (same as Pixel/SCT)
- 1 LTP
- spares



CSC TTC subsystem: Principal TTC paths



CSC TTC subsystem: Production quantities & schedules

Production quantities:

- **1 TTC crate**
- **1 single-board computer for TTC crate**
- **2 TTCvi modules**
- **1 TTCex module**
- **2 DCTPI modules**
- **1 LTP module**
- **2 fibers**
- **2 TTCrm (in TIMs)**
- **2 TIM modules** (+1 for test bench)
- **spares**

Schedule (all dates very approximate):

- **1st modules for use during development: useful 2Q03; needed 3Q03**
 - could be 1st production unit, a prototype, or a module on loan
- **remainder of modules for production system: useful 1Q04; needed 3Q04**

Questions

TTC crate:

- **Is our understanding of requirements in TTC crate correct?**
 - 1 TTCex services two TTC partitions (A: yes)
 - 1 TTCvi required per TTC partition (A: yes)
 - 1 DCTPI required per TTC partition (A: yes)
- **Software in TTC crate:**
 - Who writes “standard” software for configuration & control in TTC crate CPU?
(A: part of ROD crate DAQ)
 - Is there any “non-standard” software required in TTC crate CPU? (A: unknown)
- **Does some common development of LTP (local trigger) modules make sense?**
(A: will be investigated)

DCTPI: Who provides DCTPI? (A: LVL1 group)

TIM: Does TIM provide local Busy logic for standalone operation? (A: yes)

Spares: Who is responsible for spare modules? (A: LVL1 group)

Will there be a pool of spare modules shared by all detectors? (A: yes)